We claim:

1. A coupling system for coupling input signals from a plurality of system input ports to a system output port, comprising:

a plurality of signal amplifiers each coupled to a respective one of said system input ports;

a plurality of buffer amplifiers that are each inserted between a respective one of said signal amplifiers and said system output port, interstage junctions thus defined between said buffer amplifiers and their respective signal amplifiers;

a string of impedance elements that are each coupled between a respective pair of said interstage junctions; and

a current source coupled to provide a bias current through said string in response to activation of one of said signal amplifiers to thereby establish bias signals along said string.

2. The system of claim 1, wherein said impedance elements are resistors.

3. The system of claim 2, wherein each of said buffer amplifiers and its respective signal amplifier are arranged as a cascode amplifier stage.

4. The system of claim 1, wherein each of said signal and buffer amplifiers is realized with bipolar junction transistors.

5. The system of claim 1, wherein each of said signal and buffer amplifiers is realized with metal-oxide-semiconductor transistors.

6. The system of claim 1, wherein said signal amplifiers are differential pairs of transistors.

7. The system of claim 6, wherein each of said buffer amplifiers comprises a pair of transistors that are each arranged as a cascode

amplifier stage with a respective one of the transistors of the respective differential pair.

8. The system of claim 7, wherein said buffer amplifiers and said signal amplifiers are formed with bipolar junction transistors.

9. The system of claim 7, wherein said buffer amplifiers and said signal amplifiers are formed with metal-oxide-semiconductor transistors.

10. The system of claim 7, further including an attenuator inserted to receive said input signals and provide successively-attenuated input signals to said system input ports.

11. The system of claim 10, wherein said attenuator is a resistive ladder.

12. A coupling system for coupling input signals to a system output port, comprising:

an attenuator coupled to receive said input signals and provide successively-attenuated tap signals at a plurality of attenuator taps;

a plurality of signal amplifiers each coupled to a respective one of said taps;

a plurality of buffer amplifiers that are each inserted between a respective one of said signal amplifiers and said system output port, interstage junctions thus defined between said buffer amplifiers and their respective signal amplifiers;

a string of impedance elements that are each coupled between a respective pair of said interstage junctions; and

a current source coupled to provide a bias current through said string in response to activation of one of said signal amplifiers to thereby establish bias signals along said string.

13. The system of claim 12, wherein said attenuator is a resistive

ladder.

14. The system of claim 12, wherein said signal amplifiers are differential pairs of transistors.

15. The system of claim 14, wherein each of said buffer amplifiers comprises a pair of transistors that are each arranged as a cascode amplifier stage with a respective one of the transistors of the respective differential pair.

16. The system of claim 12, wherein each of said buffer amplifiers and its respective signal amplifier are arranged as a cascode amplifier stage.

17. The system of claim 12, wherein said impedance elements are resistors.

18. A coupling system for coupling differential input signals from a plurality of differential system input ports to a differential system output port, comprising:

a plurality of differential pairs of first and second transistors that are each coupled to a respective one of said differential system input ports;

a plurality of first buffer amplifiers that are each inserted between a first transistor of a respective one of said differential pairs and a first side of said differential system output port, first interstage junctions thus defined between said first buffer amplifiers and their respective first transistors;

a first string of impedance elements that are each coupled between a respective pair of said first interstage junctions;

a first current source coupled to provide a first bias current through said first string in response to activation of one of said signal amplifiers to thereby establish first bias signals along said first string;

a plurality of second buffer amplifiers that are each inserted

between a second transistor of a respective one of said differential pairs and a second side of said differential system output port, second interstage junctions thus defined between said second buffer amplifiers and their respective second transistors;

a second string of impedance elements that are each coupled between a respective pair of said second interstage junctions; and

a second current source coupled to provide a second bias current through said second string in response to activation of one of said signal amplifiers to thereby establish second bias signals along said first string.

19. The system of claim 18, wherein said first and second buffer amplifiers each comprise a transistor arranged to form first and second cascode amplifier stages with their respective first and second transistors.

20. The system of claim 18, further including a resistive ladder inserted to receive said differential input signals and provide successively-attenuated differential input signals to said differential pairs.